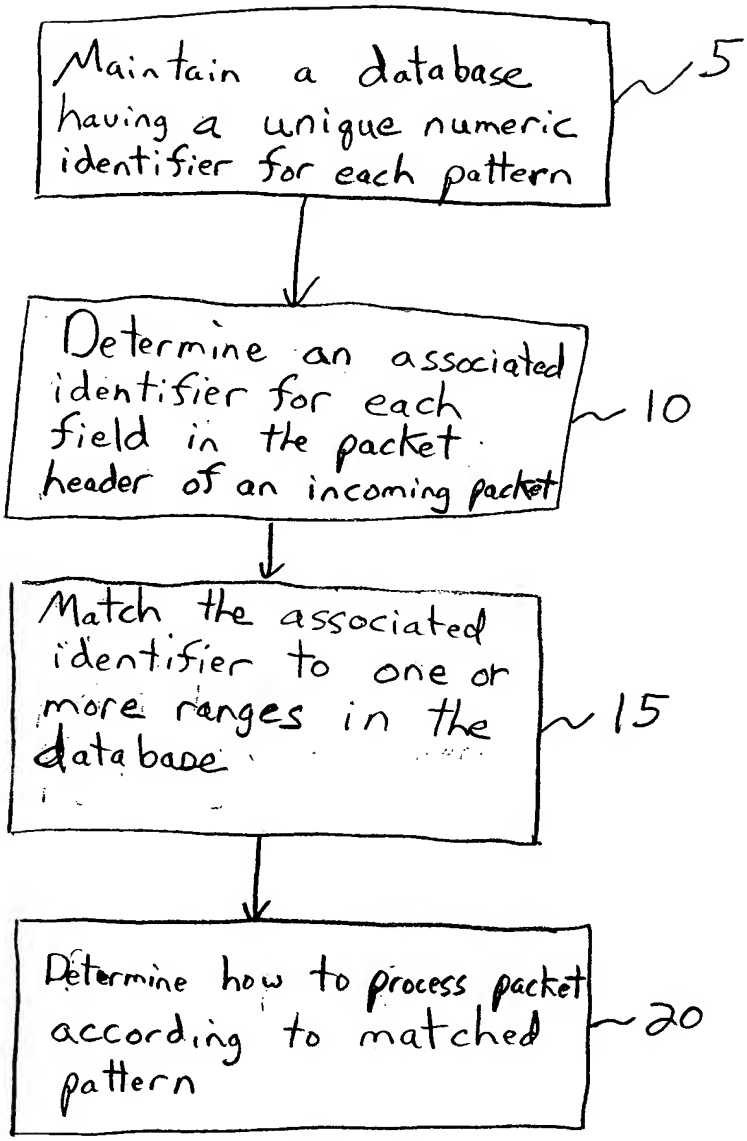

Maintain a database having a unique numeric identifier for each pattern
5
Determine an associated identifier for each field in the packet header of an incoming packet
10
Match the associated identifier to one or more ranges in the database
15
Determine how to process packet according to matched pattern
20

Fig. 1a

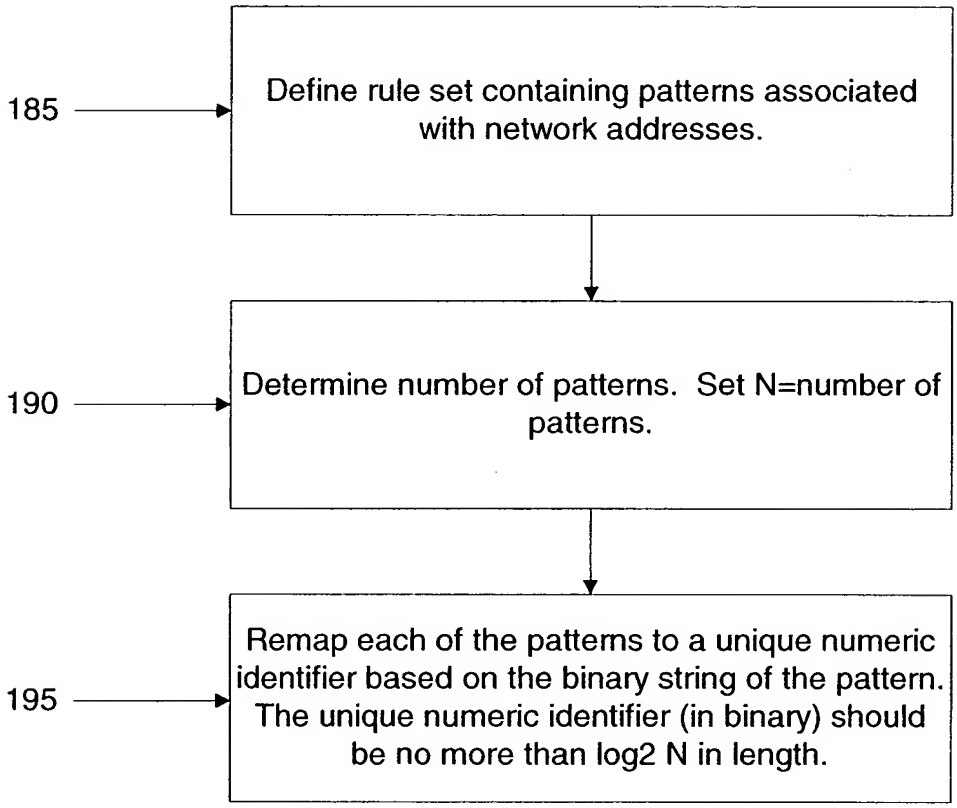

185
Define rule set containing patterns associated with network addresses.
190
Determine number of patterns. Set N=number of patterns.
195
Remap each of the patterns to a unique numeric identifier based on the binary string of the pattern. The unique numeric identifier (in binary) should be no more than log2 N in length.

Fig. 1b

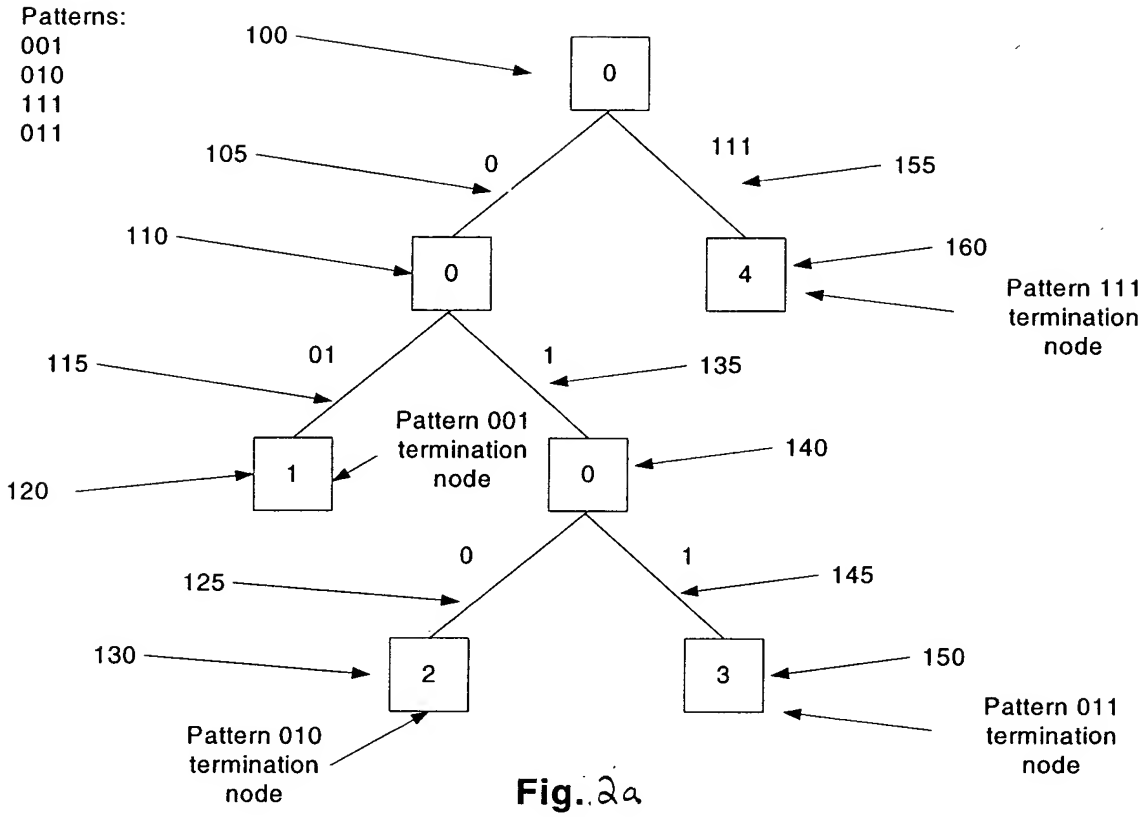

Patterns:
001
010
111
011
100
0
105
0
111
155
110
0
4
160
Pattern 111
termination
node
115
01
1
135
Pattern 001
termination
node
120
1
0
140
0
1
125
145
130
2
3
150
Pattern 011
termination
node
Pattern 010
termination
node

Fig. 2a

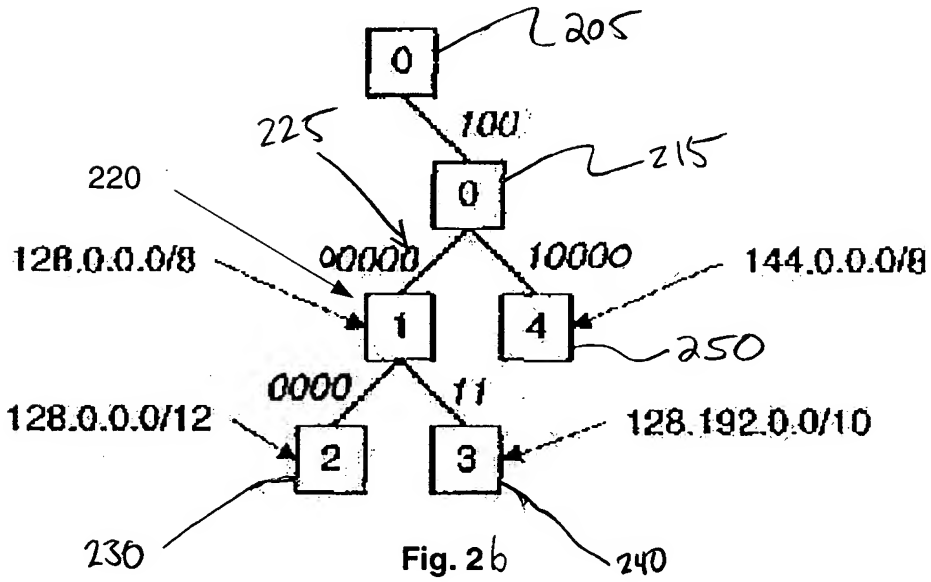

205
0
225
100
215
220
0
128.0.0.0/8
00000
10000
144.0.0.0/8
1
4
250
0000
11
128.0.0.0/12
128.192.0.0/10
2
3
230
240

Fig. 2b

300

	Pattern	Lower	Upper
310	128.0.0.0/8	1	3
320	144.0.0.0/8	4	4
330	128.0.0.0/12	2	2
340	128.192.0.0/10	3	3

Fig.3

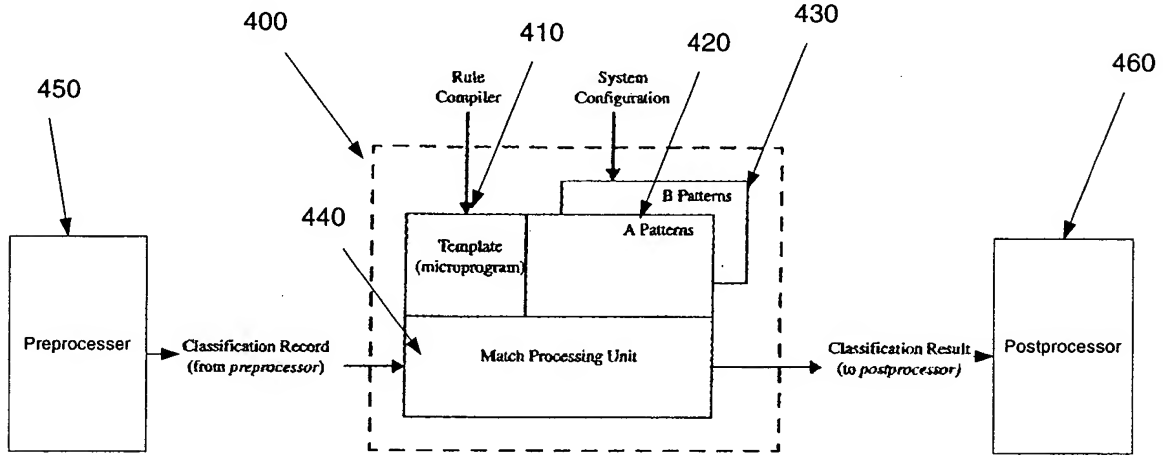


Fig. 4

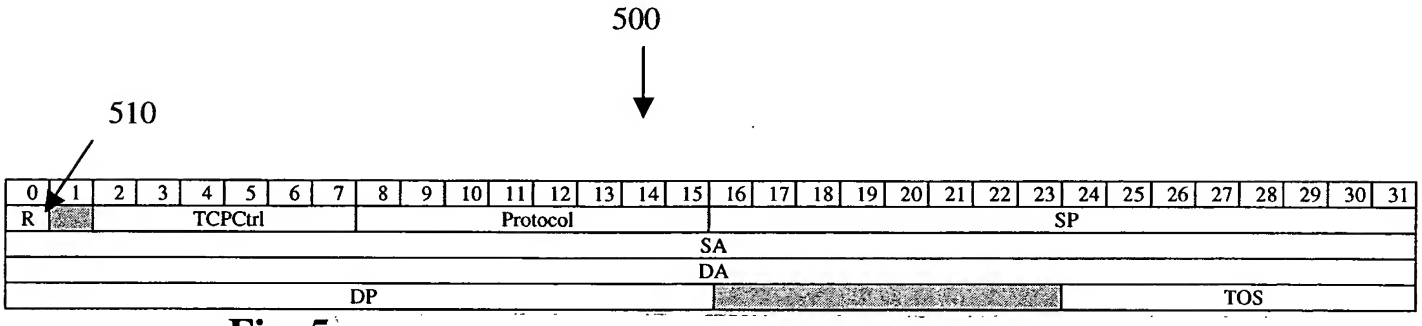


Fig. 5

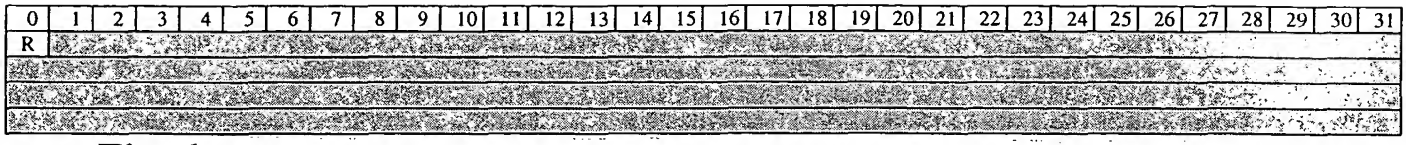


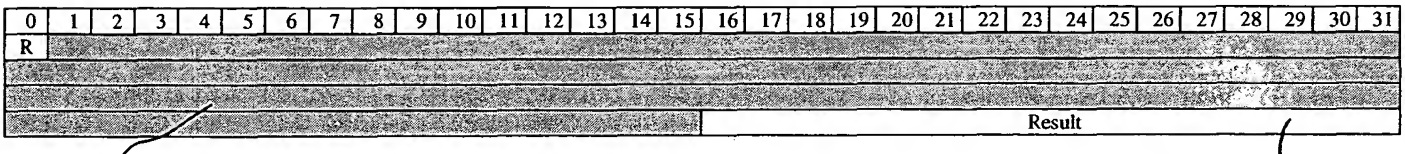
Fig. 6

710 720 730 740 750

Field	Layer	Operation	#Header Bits	#Pattern Bits	Notes
SA	3	Mask/Data	32	64	Each header bit requires a pattern mask and pattern
DA		Mask/Data	32	64	data bit.
Protocol		FieldMask/Data	8	9	The mask for these fields may be applied to all bits
TOS		FieldMask/Data	8	9	in the field simultaneously.
SP	4	Range	16	32	Since a range requires a low limit and a high limit,
DP		Range	16	32	the pattern bits must specify these limits.
TCPCtrl		Flag	6	6	A flag only requires a single pattern bit that indicates either the value of the flag is a don't care or it must be set for the rule to match.
Total			120	216	

752 754 756 758 760 772 774 776 778 780

Fig. 7



820 810

Fig. 8

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M	Set[4:0]					Filter[8:0]								

910 920 930

Fig. 9

1000

Instruction[521:0]		
Opcode[2:0]	HeaderBitSel[6:0]	Pattern[511:0]

1010 1020 1030

Fig. 10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M	Set[4:0]					Filter[8:0]								

Fig. 11

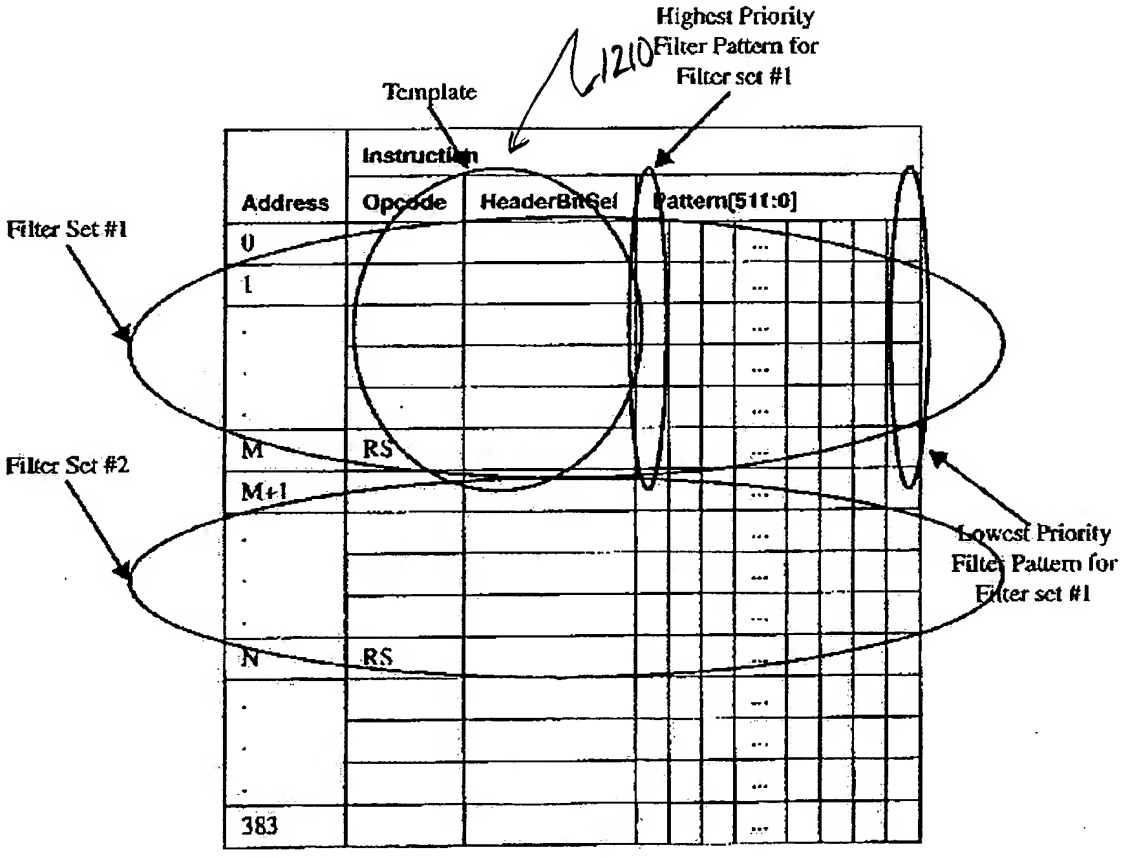


Fig. 12

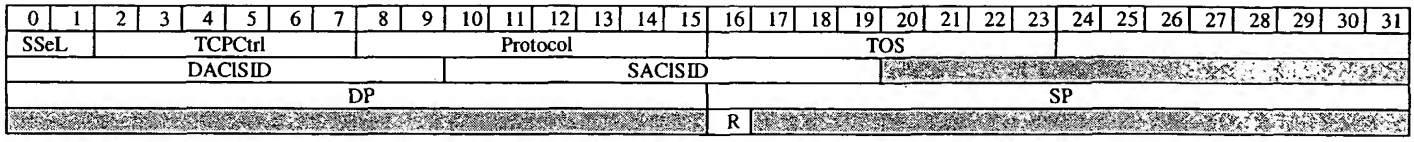

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
SSeL
TCPCtrl
Protocol
TOS
DACISID
SACISID
DP
SP
R

Fig. 13

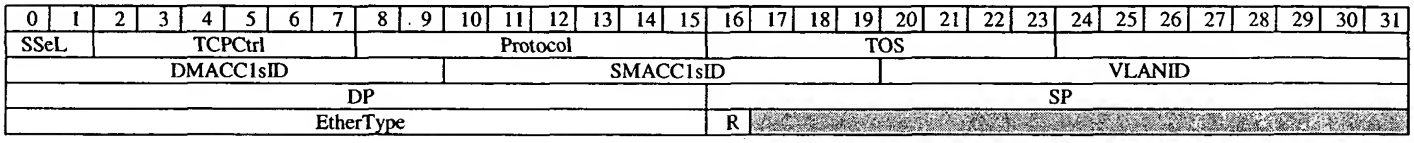

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
SSeL
TCPCtrl
Protocol
TOS
DMACC1sID
SMACC1sID
VLANID
DP
SP
EtherType
R

Fig. 14

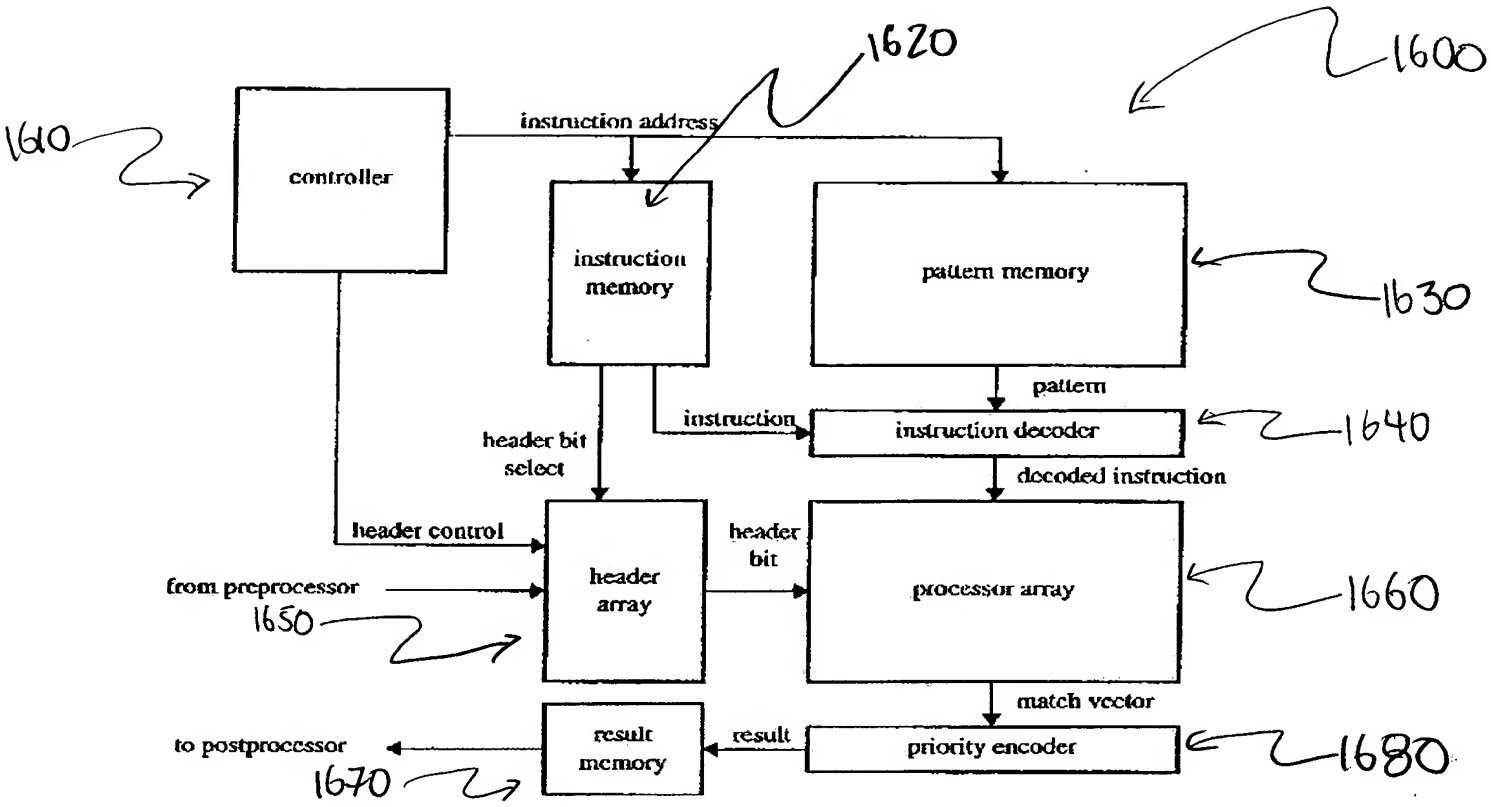

1600
1620
1610
controller
instruction address
instruction memory
pattern memory
1630
pattern
instruction
instruction decoder
1640
header bit select
decoded instruction
header control
header bit
from preprocessor
1650
header array
processor array
1660
match vector
to postprocessor
result memory
result
priority encoder
1680
1670

Fig. 15

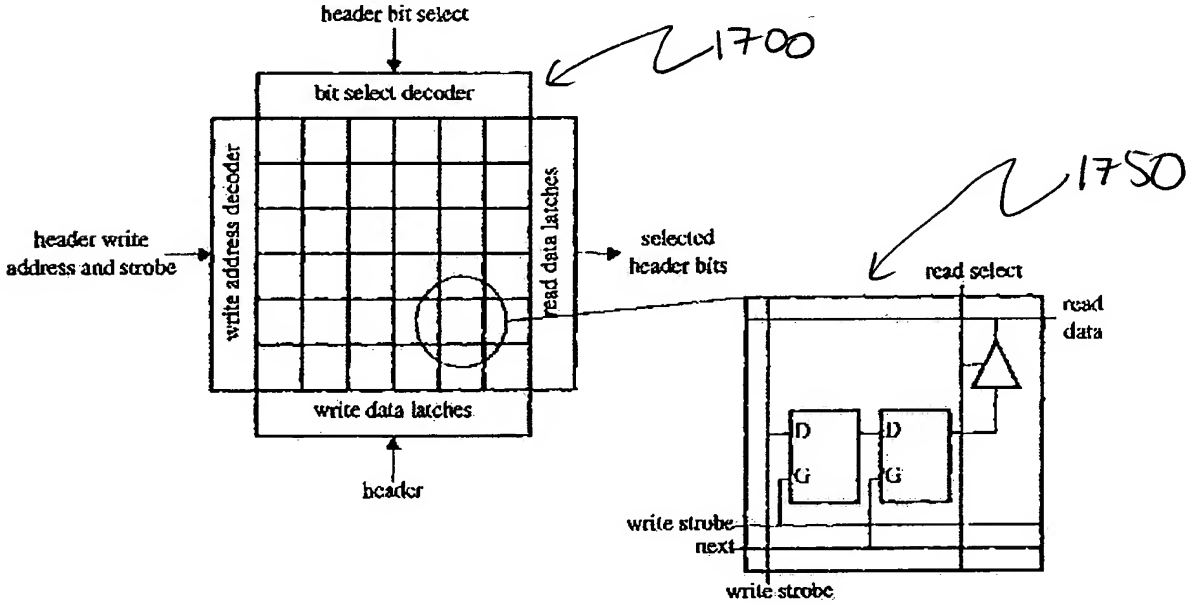

header bit select
1700
bit select decoder
write address decoder
read data latches
header write address and strobe
selected header bits
1750
read select
read data
write data latches
header
D
G
D
G
write strobe
next
write strobe

Fig. 16

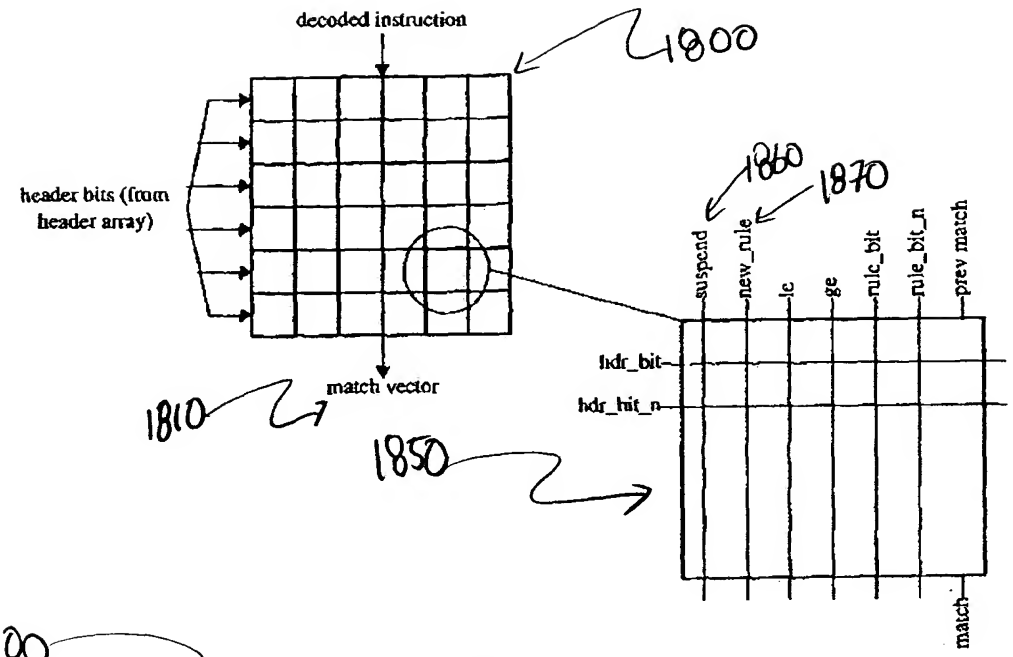

decoded instruction
1800
header bits (from header array)
1860
1870
suspend
new_rule
le
ge
rule_bit
rule_bit_n
prev match
hdr_bit
hdr_bit_n
match vector
1810
1850
match

Fig. 17

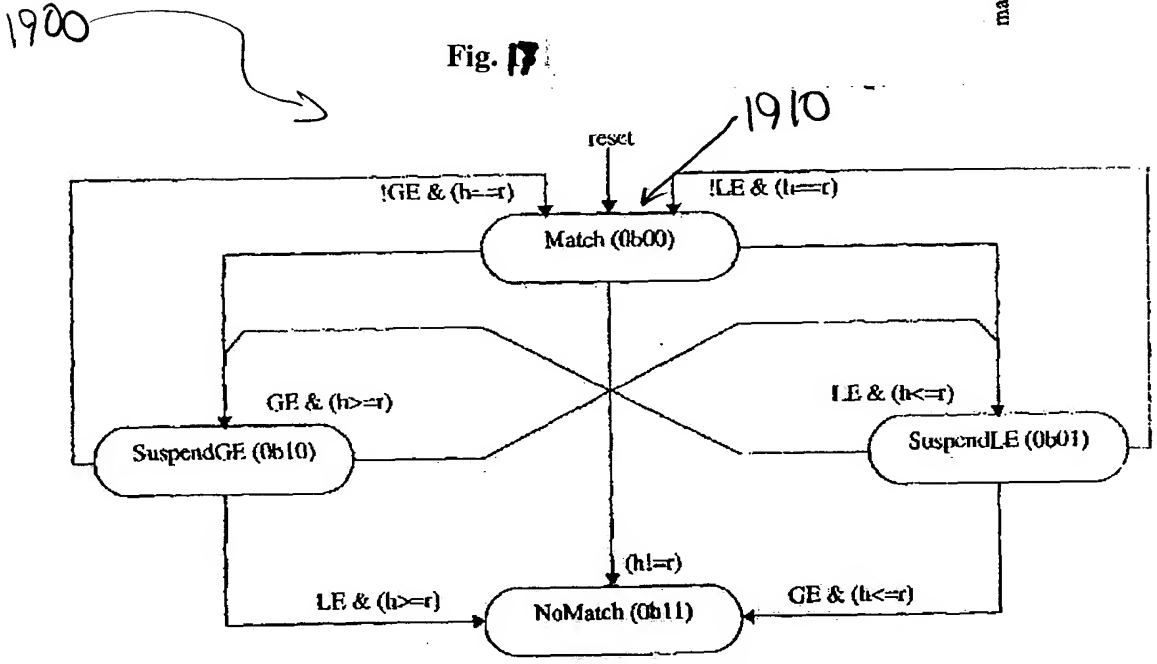

1900
1910
reset
!GE & (h==r)
!LE & (h==r)
Match (0b00)
GE & (h>=r)
LE & (h<=r)
SuspendGE (0b10)
SuspendLE (0b01)
(h!=r)
LE & (h>=r)
GE & (h<=r)
NoMatch (0b11)

Fig. 18